Multiple Voltage Systems Need Supply-Voltage Sequencing

The following application note discusses multiple solutions for sequencing power supplies and sequencing reset outputs. It discusses the advantage and disadvantages of using a discrete solution versus a more integrated solution. The MAX6819/MAX6820 provides an excellent method for sequencing multi-supply systems. The MAX6391/MAX6391 have sequenced output, which can be used for multi-voltage and/or multi-processor systems.

Many applications require a controlled cycle during power-up and power-down. For older parts that operate on bipolar supply voltages (like DG401 switches), you should apply the most positive voltage first, a logic supply (possibly) next, and the negative supply voltage last. Violating this rule can cause "latch-up" within the semiconductor.

Because external blocking diodes (added to prevent latch-up effects) can limit the usable analog input range, the preferred approach is to control the sequence in which supply voltages are applied to the chip. Controlled power sequencing is critical to the operation of many computer-oriented systems. For example, DSPs and other multivoltage microprocessors usually require their I/O voltage to be present before applying the core voltage, and vice versa. Another application that requires sequencing is a board that includes a secondary controller like a graphics controller along with the main CPU. To avoid uncontrolled outputs on the graphic display, the CPU must be up and running before the graphics controller receives power or has its reset released.

New families of ICs simplify the sequencing power to systems that require multiple supplies. We will describe these new ICs and their implementation after a discussion of discrete component approaches.

Simple RC Approach

A simple approach for sequencing the supply voltages of two or more circuits on the same rail is to simply introduce a delay between them by adding a series resistor and capacitor to ground on the power line. Only two discrete parts are required per line (Figure 1). However, this technique has many disadvantages: You should use it only for signal delays — not for power delays.
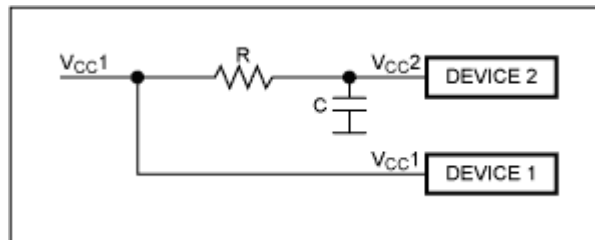

Figure 1. Power sequencing by an RC delay in the power line

Delay depends on the rise time of the supply voltage. An RC approach isn't desirable for adding delay to a 3.3V supply voltage that's independent of the primary 5V supply, because 3.3V could come up first even with the delay. The 5V may not come up at all, which doesn't prevent 3.3V from being applied to the device. This approach might be acceptable if 3.3V is derived from 5V, but you must still consider the power loss in the resistor. As another consideration, the delayed supply voltage at power-down remains applied to the load longer than does the supply voltage that came up first.

A more reliable way to prevent one supply from coming up before another is to monitor the primary supply, to ensure it comes up first and reaches a certain level before the second supply turns on. Adding a small delay provides an additional reliability advantage. Figure 2 illustrates this approach for a system in which the power regulators are located in a remote power supply for example, and are therefore not accessible.
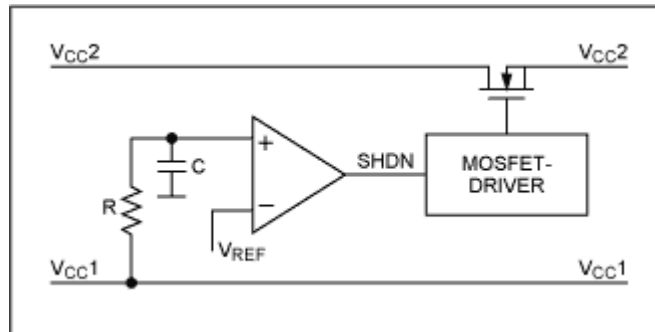

Figure 2. Power sequencing via RC , comparator, and MOSFET-driver

The reference voltage on the negative input of the comparator sets the level to be reached by Vcc - before Vcc2 turns on. An RC combination on the other input adds a delay to the trigger. An n-Channel MOSFET switch guarantees no current flows in the Vcc2 line, when power is off or when Vcc1 has not yet reached the desired voltage. To fully enhance the MOSFET switch, a driver-generated gate-source voltage (V_{GS}) exceeds Vcc2 by several volts. The simplest driver can be a charge pump that doubles Vcc2, which the comparator turns on and off via the charge pump's shutdown pin.

This approach also guarantees that Vcc2 is shut down when Vcc1 isn't present. Nevertheless, timing still depends on the rise time of Vcc1, which may not be accessible to the designer. This arrangement allows a short interval — depending on the RC combination and the fall time of Vcc1 — in which Vcc2 is present without Vcc1. As another drawback, at least five components are needed to realize this function.

An attempt to implement the above circuit with a p-channel MOSFET (to eliminate the MOSFET driver) leads to the following problems. Full closure of a PMOS device cannot be guaranteed at power-up, because rise times of the gate and source voltages can be different, or must be controlled separately. The likely result is an output glitch at power-up, before the gate-source voltage (V_{GS}) is small enough to close the MOSFET. At low voltages, additional resistance can appear in the power path because V_{GS} isn't large enough to fully enhance the p-channel MOSFET.

The circuit above can easily be upgraded with standard reset ICs, and the result is fewer external components (Figure 3). Alternatives include the MAX809 (including voltage reference, comparator, fixed delay time, and reset threshold) and the MAX6301, for which the threshold and reset time are both adjustable. However, the main advantage is a more accurately adjustable timing that's also independent of the supply voltage rise and fall times. Moreover, Vcc2 shuts down as soon as Vcc1 falls below a certain threshold, so Vcc2 is never present without Vcc1.
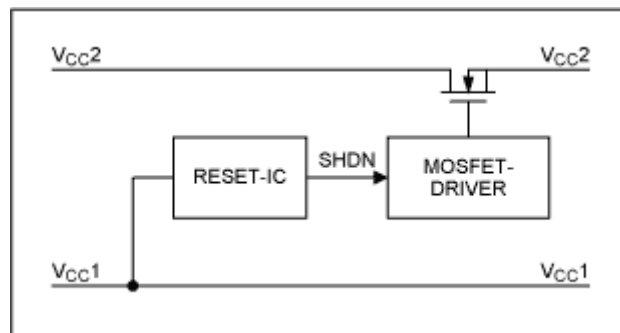

Figure 3. Sequencing with reset-IC, driver, and MOSFET

Power Regulator Sequencing

Many step-up and step-down regulators include a shutdown pin that can be used for power sequencing. First, you should examine whether the part in question fully shuts down, or whether input voltage is still present on the output (as is the case for many step-up regulators currently available). With suitable regulators, the desired sequencing can be accomplished with just an RC network on the shutdown input of one regulator (Figure 4). The RC delay ensures that Vcc1 appears before Vcc2. As for other RC circuits mentioned above, the Vcc2 delay time also depends on the Vcc1 rise time — so at power down, Vcc2 may be present longer then Vcc1.
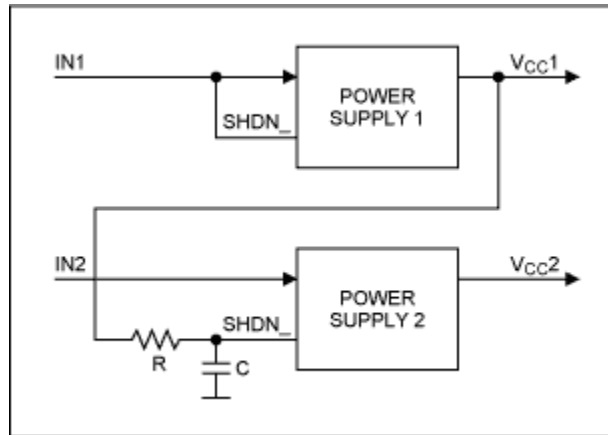

Figure 4. RC sequencing with power regulators

For better reliability, a reset IC with integrated delay can control the power regulator's shutdown pin (Figure 5). Advantages include a defined timing behavior, a controlled power-down, and a guarantee that Vcc2 shuts down before Vcc1.
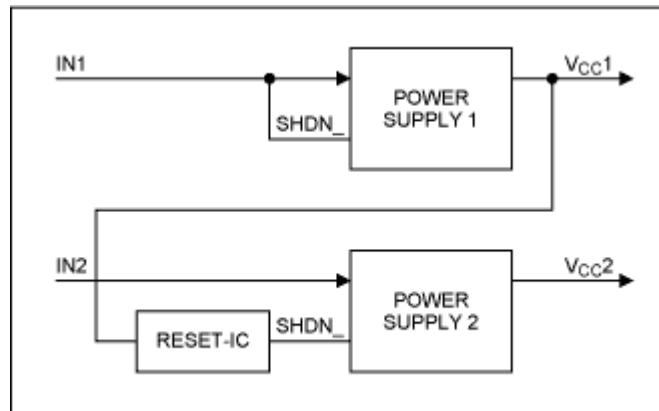

Figure 5. Reset sequencing with power regulators

With a few external components, the MAX6819 or MAX6820 offer a simple way to control the power-up/power-down cycle of various power lines on a board. While monitoring a primary supply voltage, these devices enable/disable a secondary supply voltage via an external n-channel MOSFET switch (Figure 6). The circuit functions as described above, but with much less effort. The MOSFET driver, a regulated charge pump with $V_{GS} = 5.5V$, is integrated along with the necessary capacitors in this SOT23 device.
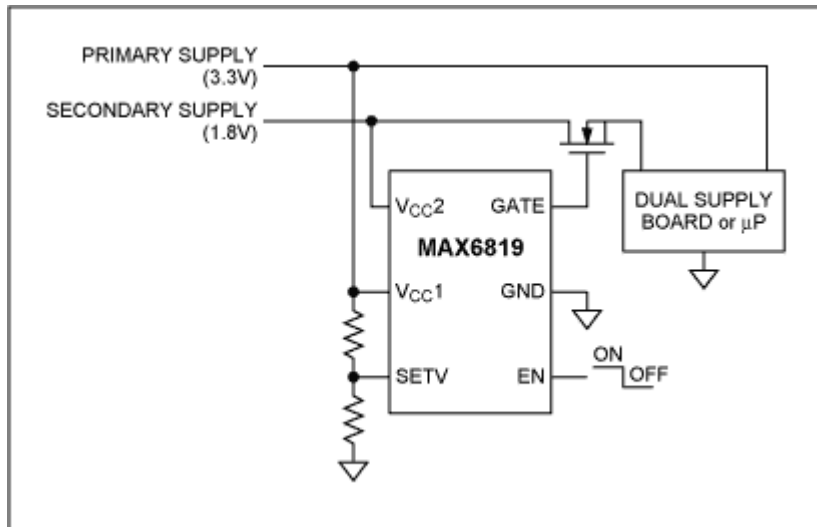
Figure 6. Power sequencing with the MAX6819

The sequencers ensure that the MOSFET always has the minimum required V_{GS} enhancement, which minimizes loss in the MOSFET and ensures a low drain-to-source impedance ($R_{DS(ON)}$). The MAX6819 imposes a factory-set delay time of 200 ms, which occurs after the primary voltage rises above the set threshold and before enabling the charge pump to drive the external MOSFET switch.

The MAX6819 also has an Enable input that can override the internal circuitry and shut down or enable the external MOSFET. The MAX6820 allows users to simply adjust the delay time with a small external capacitor. Provided one supply is greater than 2.125V, either Vcc1 or Vcc2 can act as the primary source and thereby trigger the switch for the secondary supply.

Because some systems must sequence more than two supplies, the MAX6819 and MAX6820 support daisy chaining (Figure 7). All upstream power switches are disabled as long as power supplies upstream of the switches haven't reached their proper operation voltage, and the relevant delay time hasn't passed.
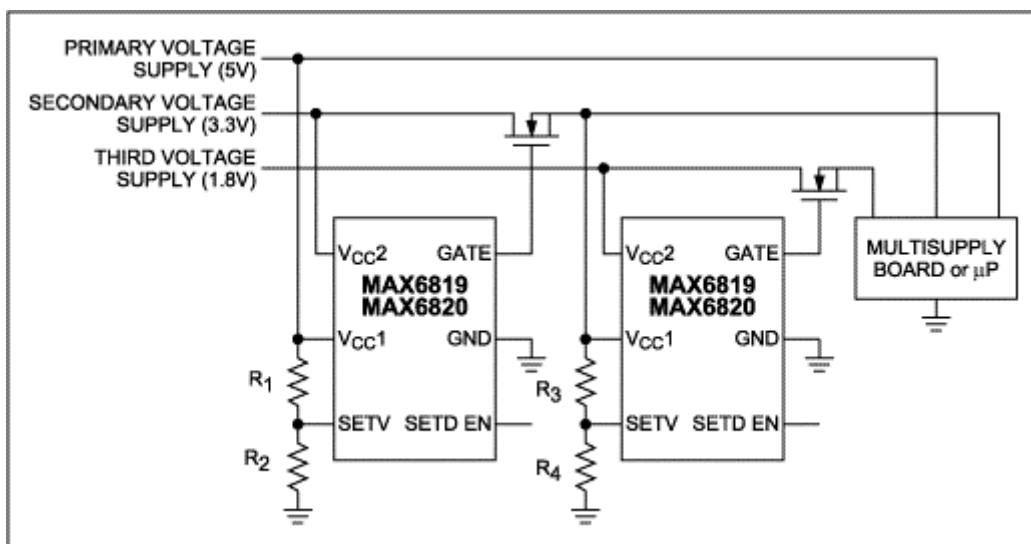

Figure 7. Sequencing three power supplies

Reset Sequencing

If you must control the reset timing rather than the power supply, you need a reset sequencer. This capability is necessary if, for example, a master CPU must be up and running before a slave CPU or a backplane ASIC. You can achieve the required sequencing by cascading two or more reset ICs like the MAX812, which include a manual reset input (MR). When the first supply voltage is up, and the first reset IC pulls its reset output high, the MR of the second IC is released and the internal timer starts running. After the delay time passes, the second reset is then deasserted.

The same function with some additional flexibility is provided in a single chip by the new MAX6391/MAX6392 dual-voltage µP-supervisory circuits with sequenced outputs (Figure 8). These SOT23-8 parts monitor two supply voltages (master and slave), and provide two reset outputs with fixed or adjustable timeout periods.
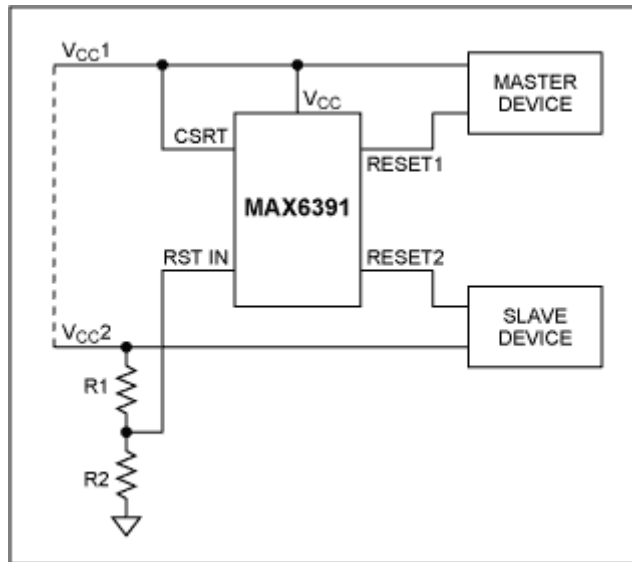

Figure 8. Reset sequencing with the MAX6391/MAX6392

The chip asserts both resets when the master supply drops or hasn't reached its operating voltage. As long as the master reset is asserted, the slave reset can't be deasserted. At power-up and power-down, the sequenced reset outputs ensure that the slave part is never turned on when the master part isn't running. The voltage threshold and timeout period for the slave device are adjustable with a few external components. A similar version of this article appeared in the April 2002 issue of *Power Electronics* magazine.

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MORE INFORMATION

MAX6301:	QuickView	-- Full (PDF) Data Sheet (112k)	-- Free Sample
MAX6391:	QuickView	-- Full (PDF) Data Sheet (176k)	-- Free Sample
MAX6392:	QuickView	-- Full (PDF) Data Sheet (176k)	-- Free Sample
MAX6819:	QuickView	-- Full (PDF) Data Sheet (216k)	-- Free Sample
MAX6820:	QuickView	-- Full (PDF) Data Sheet (216k)	-- Free Sample
MAX809:	QuickView	-- Full (PDF) Data Sheet (176k)	-- Free Sample

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